### Stability and Phase Margins

- **Gain Margin**: change in open-loop gain (dB) at 180° to make closed-loop system unstable

- **Phase Margin**: change in open-loop phase shift at unity gain to make closed-loop system unstable

### Close-loop Transient vs. Frequency Response

- Recall, 2nd order-system

\[
MP = \frac{1}{2\zeta \sqrt{1 - \zeta^2}}
\]

\[
\omega_p = \omega_n \sqrt{1 - 2\zeta^2}
\]

### Phase Margin via Damping Ratio

- Consider the 2nd order open-loop TF

\[
G(s) = \frac{\omega_n^2}{s(s + 2\zeta \omega_n)}
\]

- Compute the Phase Margin, \(\phi_M\):

\[
\phi_M = \tan^{-1} \frac{2\zeta}{\sqrt{-2\zeta^2 + \sqrt{1 + 4\zeta^4}}}
\]

### Bandwidth of a System

- Frequency at which magnitude of response curve is 3dB below its value at 0 rad/s

\[
\omega_{BW} = \omega_n \sqrt{1 - 2\zeta^2 + \sqrt{4\zeta^4 - 4\zeta^2 + 2}}
\]
Steady-State Error

Unit Step Input
\[ e(\infty) = \lim_{s \to 0} \frac{1}{1 + sG(s)} \]
Position Constant
\[ K_p = \lim_{s \to 0} G(s) \]
Ramp Input
\[ e(\infty) = \lim_{s \to 0} \frac{1}{sG(s)} \]
Velocity Constant
\[ K_v = \lim_{s \to 0} sG(s) \]
Parabolic Input
\[ e(\infty) = \lim_{s \to 0} \frac{1}{s^2G(s)} \]
Acceleration Constant
\[ K_a = \lim_{s \to 0} s^2G(s) \]

Bode Plots & Steady-State Error Constants

\[ K_p \]
\[ 20 \log |K_p| \]
\[ 20 \log |s| \]
\[ -20 \log |s| \]
\[ -20 \log |s| \]

General Frequency Response Design Guidelines

- Open-loop stable system is closed-loop stable if Mag-Freq response has gain less than 0 dB at the pt where the Phase-Freq response is 180°
- OS% is reduced by increasing \( \Phi_M \)
- Speed of response is increased by increasing \( \omega_N \)
- \( \Theta_{ess} \) is improved by increasing low-freq magnitude response even if high-freq response gets attenuated

Lag Compensation

- Passive analog of PI controller
- Improves steady-state error by increasing high frequency gain
- Increases phase margin to obtain desired transient response
Design Procedure for Lag Compensator

\[ G_c(s) = \frac{s + \frac{1}{\alpha T}}{s + \frac{1}{\omega_n}} \]

1. Set K to satisfy steady-state specification & plot Bode diagrams for selected K
2. Find \( \omega_d \) where \( \Phi_M \) is 5º-12º greater than \( \Phi_M(\zeta_d) \)
3. Set |\( G_c(j\omega) \)| s.t Bode plot for \( G_c(j\omega)G(j\omega) \) goes through 0dB at \( \omega_d \)
4. Set upper break freq. @ 1 decade below \( \omega_d \)
5. Low freq. asymptote to be at 0 dB
6. Connect low + high freq. asymptote via -20 dB/decade line to locate low break freq.
7. Reset K to compensate for any attenuation from \( G_c \) to maintain steady-state specs

Example

Let \( G(s) = \frac{100K}{s(s+36)(s+100)} \). Design a lag compensator s.t. we achieve a 10 fold improvement in steady-state error w/ 9.5% overshoot.

Example 2

Design lag compensator w/ \( K=2 \) for 11% overshoot and improve \( e(\infty) \) by a factor of 30.

Lead Compensation

- Passive analog of PD compensation
- Cascade compensator

\[ G_c(s) = \frac{1}{\beta T} \frac{s}{\beta s + 1} \]
The Effects of a Lead Compensator

Frequency Response of the Lead Compensator

- Determine \( M_c(\omega) \) & \( \phi_c(\omega) \), given

Design Procedure for Lead Compensation

1. Find closed-loop bandwidth requirement to meet \( T_s \), \( T_p \) or \( T_r \)
2. Set \( K \) s.t. uncompensated system satisfies steady-state error specs
3. Plot Bode plots for set \( K \) and determine uncompensated system's phase margin
4. Find phase margin to meet \( \zeta \) or \%OS, find phase contribution from \( G_c \)
5. Determine \( \beta \)
6. Determine \( |G_c(j\omega)| \) @ peak of phase curve
7. Determine phase margin \( \phi \)
8. Design the break frequency for \( G_c \)
9. Reset system gain to compensate for \( G_c \)'s gain
10. Check bandwidth to ensure Step 1 specs are met
11. Simulate to check
12. Redesign if needed

Example 3

Given \( G(s) = \frac{100K}{(s(s+36)(s+100))} \), design a lead compensator s.t. \%OS = 20\%, \( T_p = 0.1s \), and \( K_r = 40 \).
Example 4
Given \( G(s) = \frac{K}{(s(s+50)(s+120))} \), design a lead compensator s.t. \%OS = 20%, \( T_S = 0.2s \), and \( K_v = 50 \).

PI Compensation w/ Bode Plots
\[
G_C(s) = K_1 + \frac{K_2}{s} = \frac{K_1 s + \frac{K_2}{s}}{s}
\]
1. Set \( K \) to meet steady-state spec
2. Determine the phase contribution of \( G_c \) and thus \( \Phi_{M,comp} \)
3. Plot Bode plots for \( G(s) \) for \( K \) chosen in Step 1
4. Find \( \omega \) and magnitude (dB) s.t. phase angle is \(-180^\circ + \Phi_{M,comp}\)
5. Set break freq. to be 0.1 \( \omega \)
6. Set \( K_i \) s.t. magnitude of response is 0 dB at \( \omega \)

Example
Design PI controller to yield 0 steady-state error for a ramp input and 9.48% overshoot for a step input.

PD Compensation w/ Bode Plots
\[
G_C(s) = K_1 + K_2 s = \frac{K_1(s + \frac{1}{K_2})}{s}
\]
1. Find closed-loop \( \omega_{WB} \) to meet \( T_P, T_r, \) or \( T_s \)
2. Set \( K \) to meet steady-state
3. Pick the \( \omega_{WB,new} = \omega_{WB} + \omega_{correction} \) where \( \omega_{correction} \) is set by the designer
4. Find the phase angle at the new \( \omega_{WB,new} \) (given in 3)
5. Find the contribution of the compensator = \(-180^\circ + \Phi_{M,comp}\) + \( \Phi_{M_d} \)
6. Determine \( K_v/K_2 \) based on the angle found in 5
7. Set \( K_2 \) such that DC gain of compensator is unity